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09/608,624	06/30/2000	Stephen Jourdan	2207/8609	9451

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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/608,624	JOURDAN ET AL.	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9-19,22-27 and 39-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-7,9-15 and 17-19* is/are allowed.

6)☒ Claim(s) *2,3,16,22-26 and 39-43* is/are rejected.

7)☒ Claim(s) *27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 3, 16, 22-26 and 39-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peled et al. (U.S. Patent No. 6,076,144), hereinafter referred to as Peled in view of Stepanov et al. (The Standard Template Library) herein referred to as Stepanov.

3. Referring to claim 3, Peled discloses as claimed: a memory entry (Data Array 200; see Figure 3 and Figure 11; see col. 3, lines 30-35), storing a trace (Basic Block B, see Figures 11 and 12; col. 14, lines 10-18) having a multiple-entry (LA2 and LA2'; see Figure 12;col. 14, lines 32-42 and 54-67; col. 15, lines 1-2), single exit (Last instruction in the B Block; B9; see Figure 11) architecture.

4. Peled does not expressly disclose the entry is indexed by an address of a terminal instruction therein.

5. Stepanov teaches indexing a data structure by the terminal entry (see page 22 regarding a.back() which addresses a container by its last entry).

6. It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the system of Peled by indexing the address of a terminal instruction within the trace, as taught by Stepanov. The choice to address from the front of a structure or the back is merely a design choice. Additionally, since there are only two possibilities (addressing from the first or the last entry), it would have obvious for one of ordinary skill in the art to have done either.

Referring to claim 16, Peled discloses as claimed: A processing engine (As shown in Figure 1), comprising: a front end stage (Stage including TBPU 110; see Figure 1) to store blocks (Such as block B for example; see col. 14, lines 32-48), of instructions in a multiple-entry (LA2 and LA2', see above regarding claim 1), single exit (Instruction B9; see above regarding claim 1) architecture when considered according to program flow, and an execution unit (Execution units 125; see Figure 1) in communication with the front end stage (See Figure 1).

Peled does not expressly disclose the entry is indexed by an address of a terminal instruction therein.

Stepanov teaches indexing a data structure by the terminal entry (see page 22 regarding a.back() which addresses a container by its last entry).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the system of Peled by indexing the address of a terminal instruction within the trace, as taught by Stepanov. The choice to address from the front of a structure or the back is merely a design choice. Additionally, since there are only

two possibilities (addressing from the first or the last entry), it would have obvious for one of ordinary skill in the art to have done either.

Referring to claim 22, Peled discloses as claimed: apparatus, comprising a memory entry storing (See Figure 12; see above regarding claim 1) a sequence of program instructions (Instructions B1-9) as a trace (See col. 1; lines 50-60), the instructions defining a program flow that progresses (See col. 14; lines 35-45) from any instruction (All instructions B1-B8 will flow to instruction B9) therein to a last instruction (Instruction B9; see above regarding claim 1) in the trace and in which the trace has multiple separate prefixes (LA2 and LA2'; see above regarding claim 1).

Peled does not expressly disclose the entry is indexed by an address of a terminal instruction therein.

Stepanov teaches indexing a data structure by the terminal entry (see page 22 regarding a.back() which addresses a container by its last entry).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the system of Peled by indexing the address of a terminal instruction within the trace, as taught by Stepanov. The choice to address from the front of a structure or the back is merely a design choice. Additionally, since there are only two possibilities (addressing from the first or the last entry), it would have obvious for one of ordinary skill in the art to have done either.

Referring to claim 23, Peled discloses as claimed: a memory comprising storage for a pluralitya plurality of traces (See col. 1; lines 50-60)

Peled does not expressly disclose the entry is indexed by an address of a terminal instruction therein.

Stepanov teaches indexing a data structure by the terminal entry (see page 22 regarding a.back() which addresses a container by its last entry).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the system of Peled by indexing the address of a terminal instruction within the trace, as taught by Stepanov. The choice to address from the front of a structure or the back is merely a design choice. Additionally, since there are only two possibilities (addressing from the first or the last entry), it would have obvious for one of ordinary skill in the art to have done either.

Referring to claim 40, Peled discloses as claimed: a memory (Data Array 200; see Figure 3 and Figure 11; see col. 3, lines 30-35) having at least one memory entry (Entries in Data Array 200; see Figure 3) to store a trace having a multiple entry (LA2 and LA2'; see Figure 12;col. 14, lines 32-42 and 54-67; col. 15, lines 1-2), single exit (Last instruction in the B Block; B9; see Figure 11) architecture.

Additionally, note that what the block is intended "to store" is immaterial. Therefore, the limitation, "a trace having a multiple entry, single exit architecture" does not provide any patentable weight.

Peled does not expressly disclose the entry is indexed by an address of a terminal instruction therein.

Stepanov teaches indexing a data structure by the terminal entry (see page 22 regarding a.back() which addresses a container by its last entry).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the system of Peled by indexing the address of a terminal instruction within the trace, as taught by Stepanov. The choice to address from the front of a structure or the back is merely a design choice. Additionally, since there are only two possibilities (addressing from the first or the last entry), it would have obvious for one of ordinary skill in the art to have done either.

Claims 41-43 recite equivalent limitations as claim 40 and are rejected for the same reasons.

As to claims 2 and 39, Peled also discloses: the trace being a complex trace (The trace has multiple entry points making it more complex than one with a single entry point) having multiple independent prefixes (LA2 and LA2'; see above regarding claim 1) and a common, shared suffix (Instruction B9; see above regarding claim 1).

Additionally note that in claim 39, "a trace is a complex trace having multiple independent prefixs and a common, shared suffix" to be stored is immaterial and the claim fails to further limit the subject matter from claim 38.

As to claim 24, Peled also discloses the traces include a plurality of instructions assembled according to program flow (See col. 14; lines 35-45).

As to claim 25, Peled also discloses the traces have a multiple entry (LA2 and LA2'; see Figure 12;col. 14, lines 32-42 and 54-67; col. 15, lines 1-2), single exit (Last instruction in the B Block; B9; see Figure 11) architecture.

As to claim 26, Peled also discloses having separate prefixes (LA2 and LA2'; see above regarding claim 1) and a common suffix (Instruction B9; see above regarding claim 1), when considered according to program flow.

Allowable Subject Matter

Claims 4-7, 9-15 and 17-19 are allowed.

Claim 27 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE R. MOLL whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

/J. R. M./

Examiner, Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181